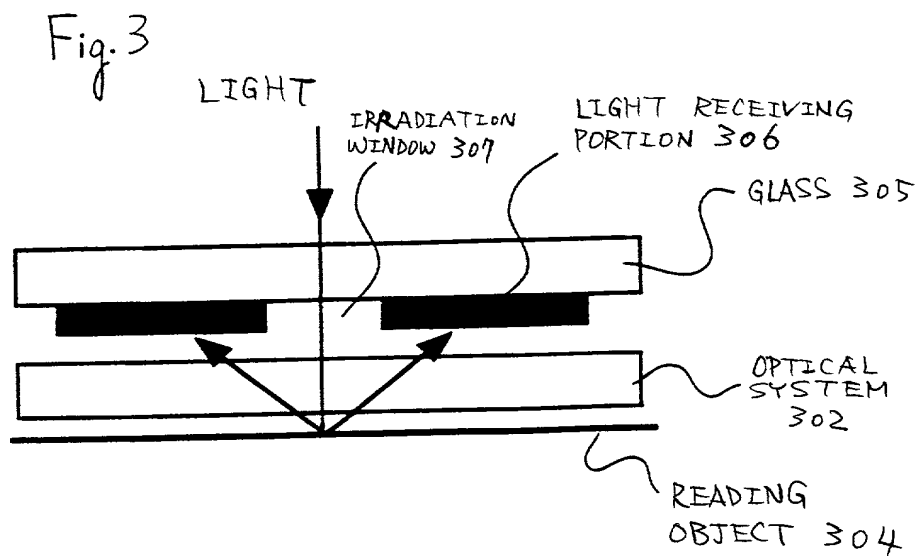
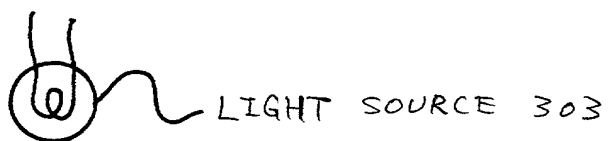
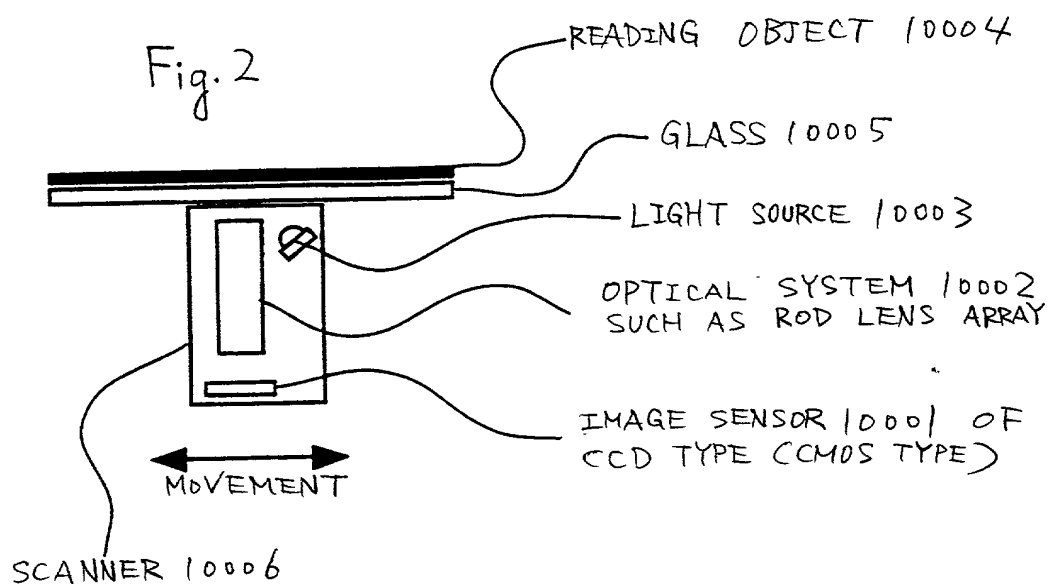


Fig. 1



[illegible]

WIRING 401

WIRING 401

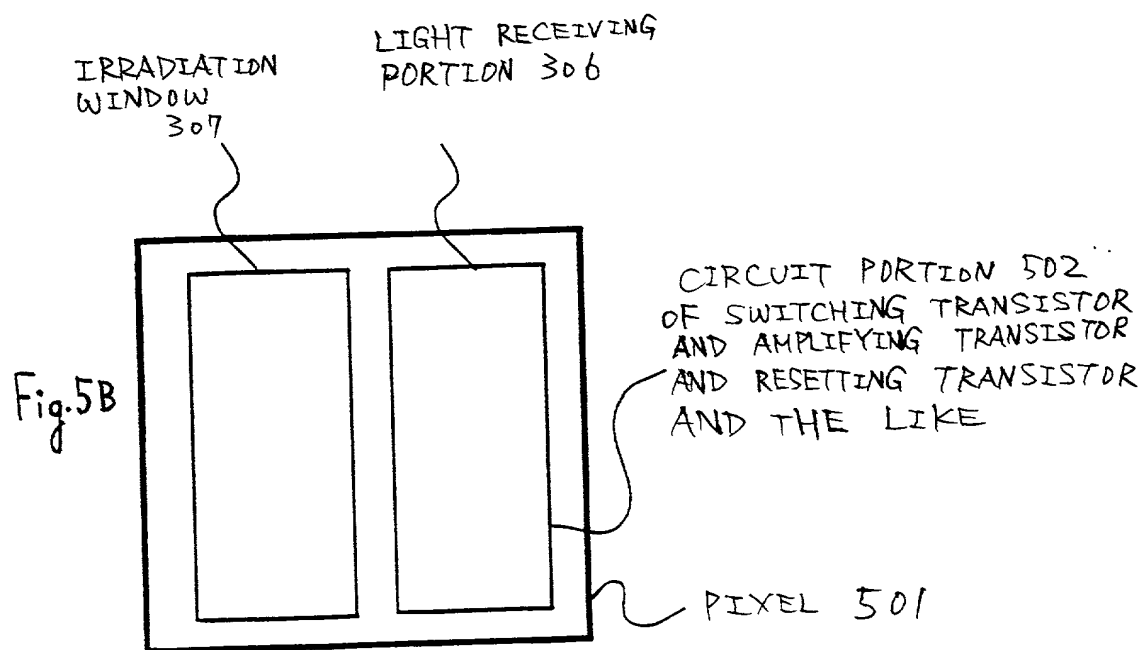
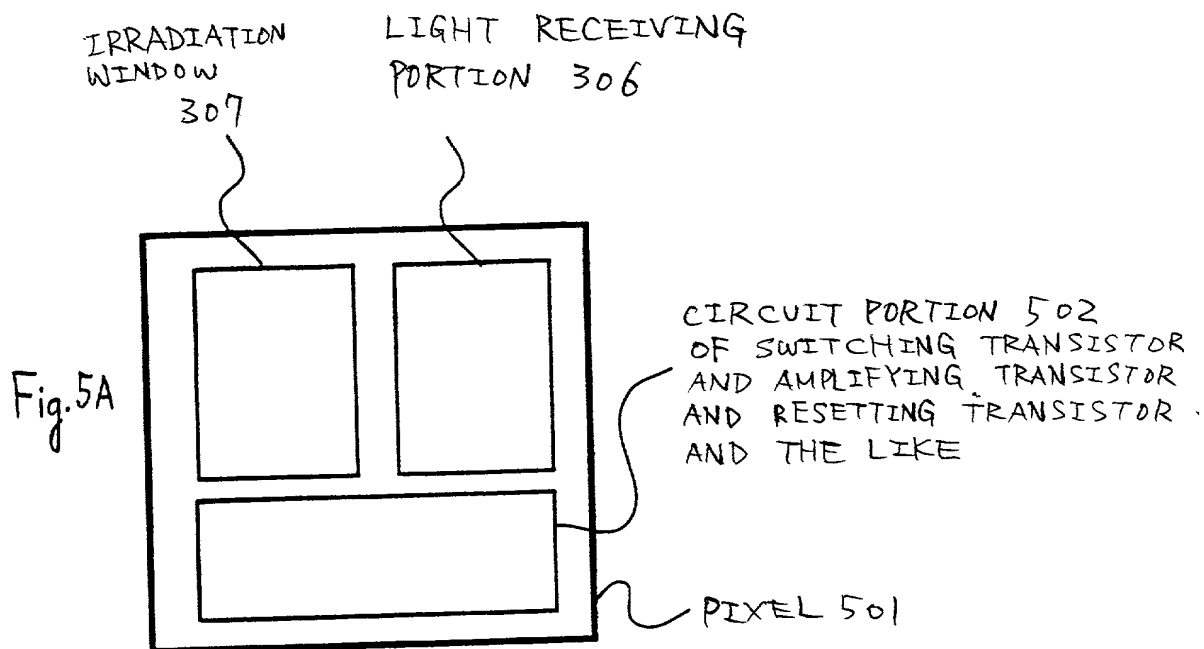
WIRING 401

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100

WIRING 401

WIRING 401

WIRING 401



INCIDENT LIGHT
FROM ARBITRARY
DIRECTION
(INDEPENDENT OF
INCIDENT ANGLE)

INCIDENT
LIGHT 601

REFLECTED
LIGHT
602

REFLECTION ANGLE: θ

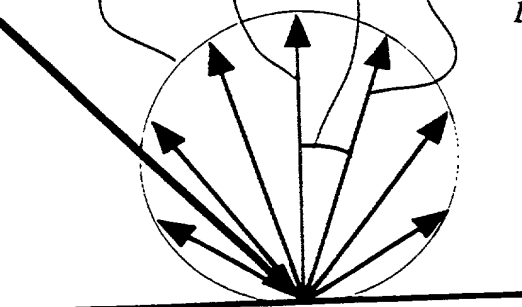
OPTICAL INTENSITY $I(\theta)$
OF REFLECTED LIGHT
HAVING REFLECTION
ANGLE OF θ

$$I(\theta) = I_0 \cos \theta$$

OPTICAL INTENSITY I_0
OF REFLECTED LIGHT
HAVING REFLECTION
ANGLE OF 0

REFLECTING FACE 603

Fig. 6



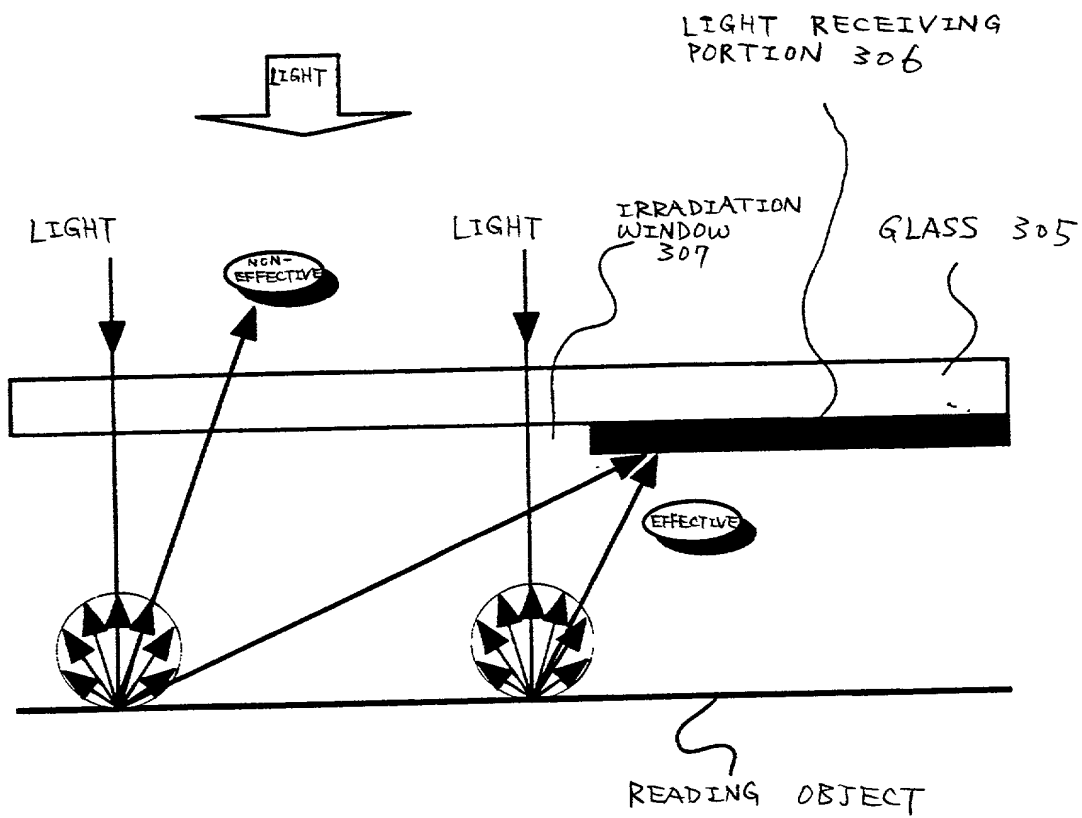


Fig. 7

LIGHT RECEIVING PORTION 806

IRRADIATION
WINDOW 807

A

A'

SECTION
LINE 801

Fig. 8

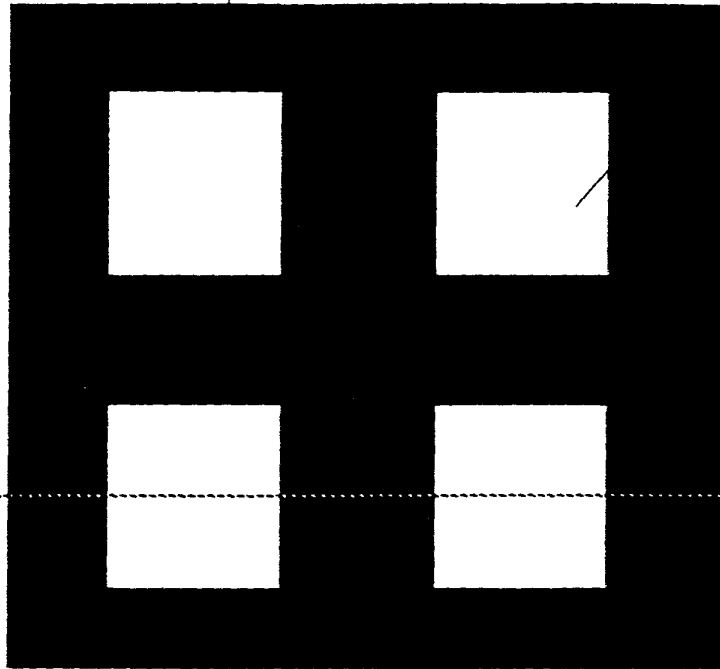
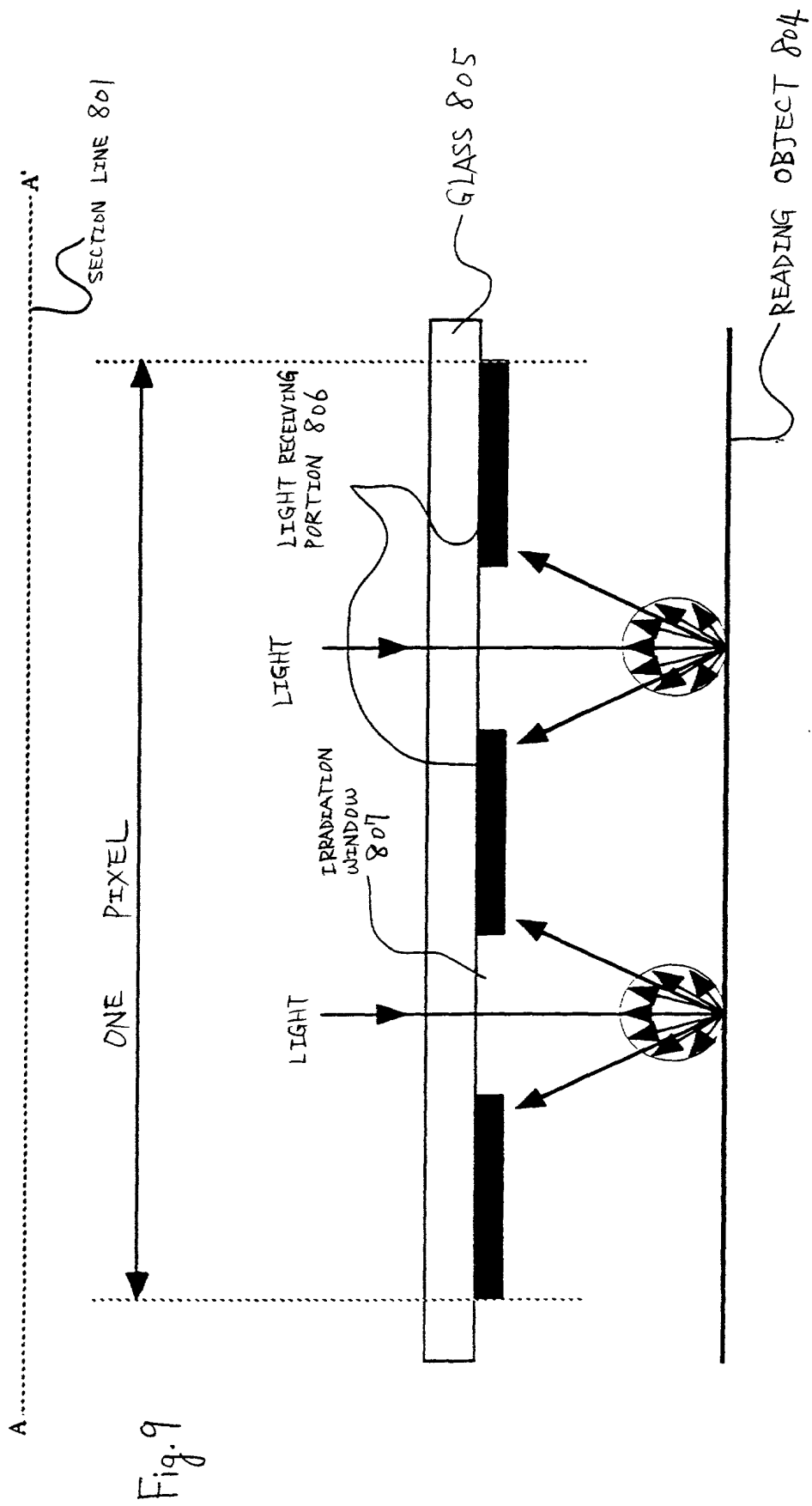
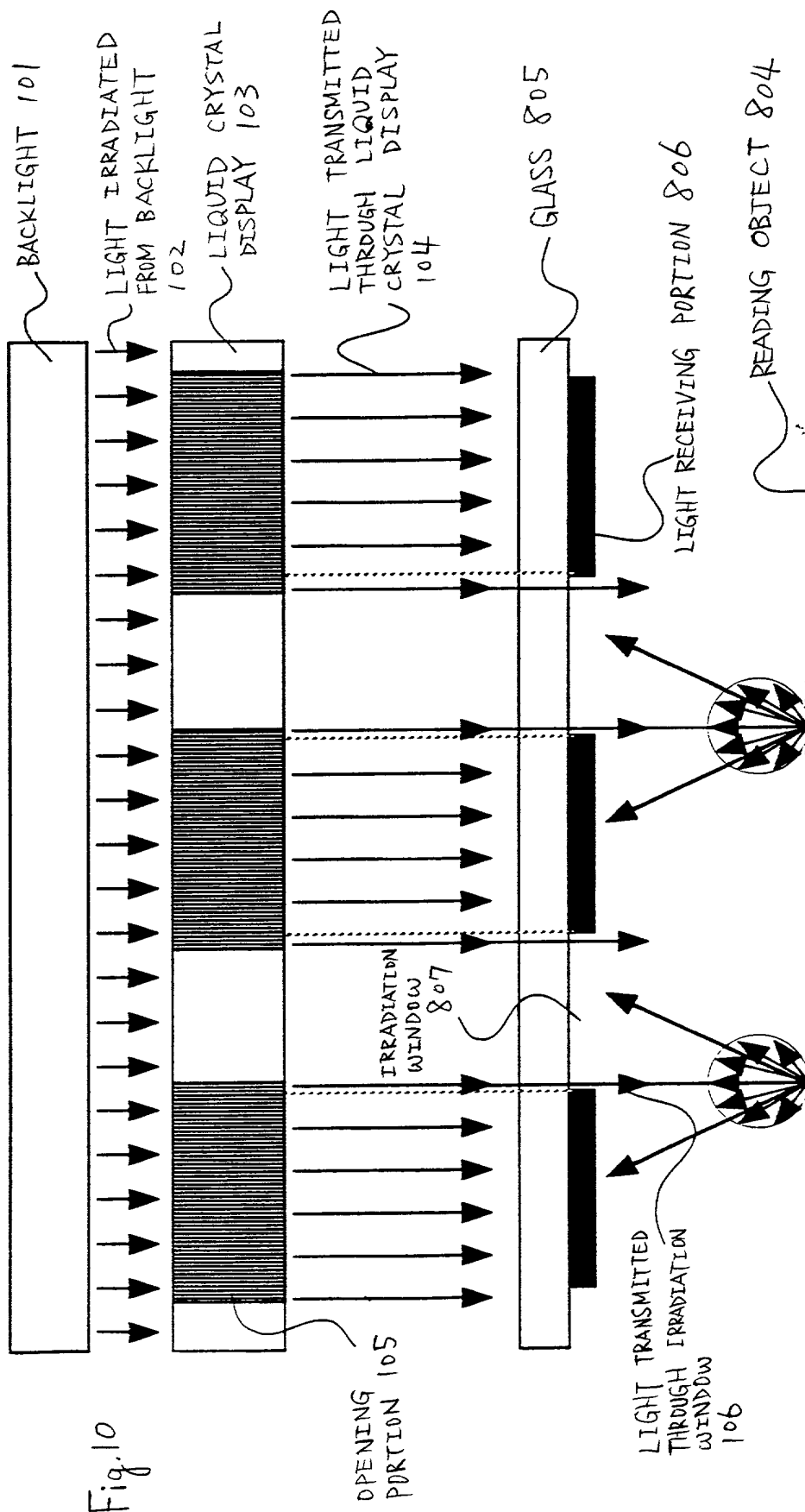


FIG. 9 is a schematic diagram of a reading device in accordance with the present invention. The device includes a reading object 804, a glass 805, an irradiation window 807, a light receiving portion 806, and a section line 801. The device is shown in a cross-sectional view along section line A-A'.





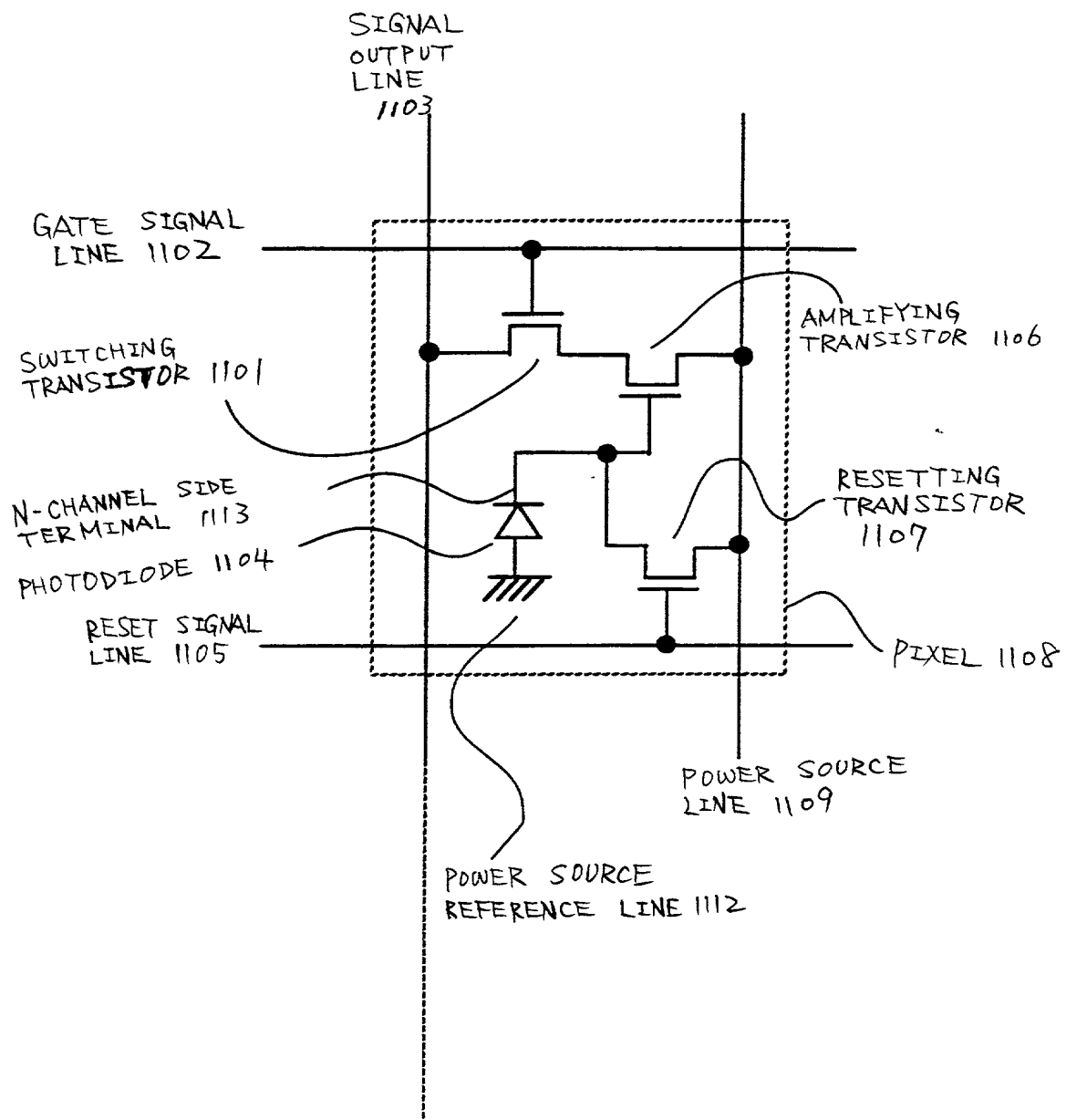


Fig. 11

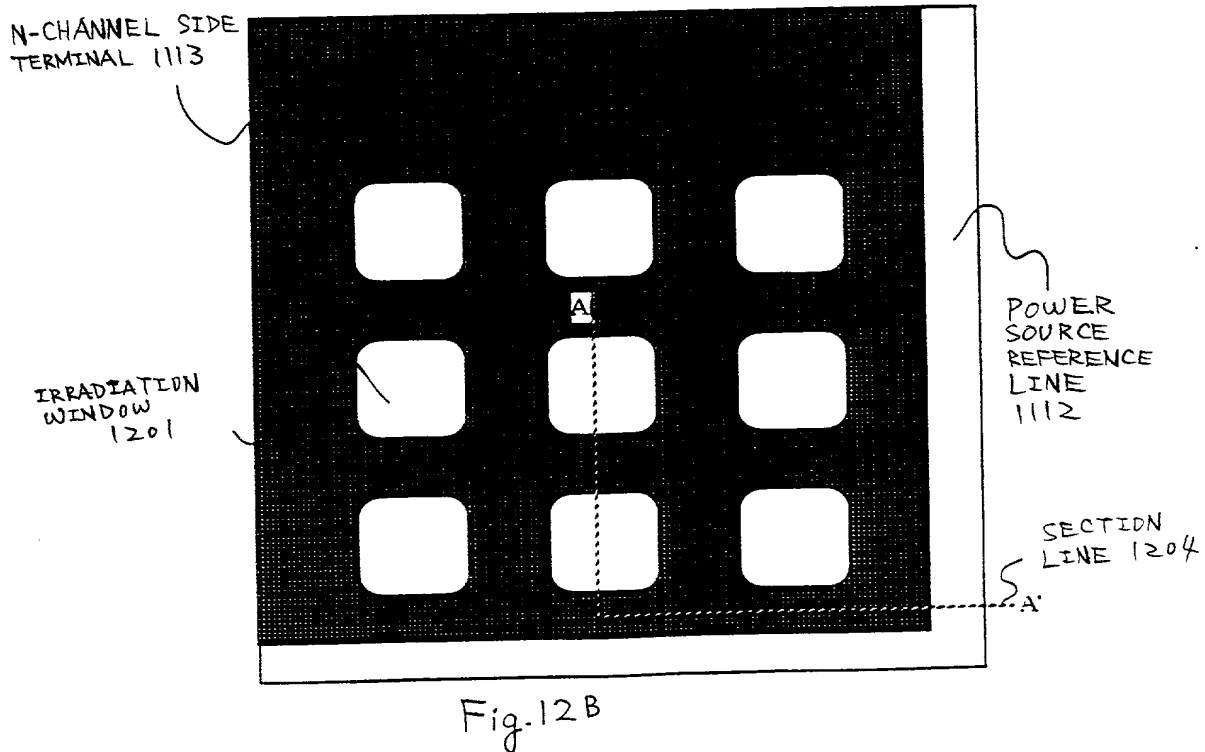
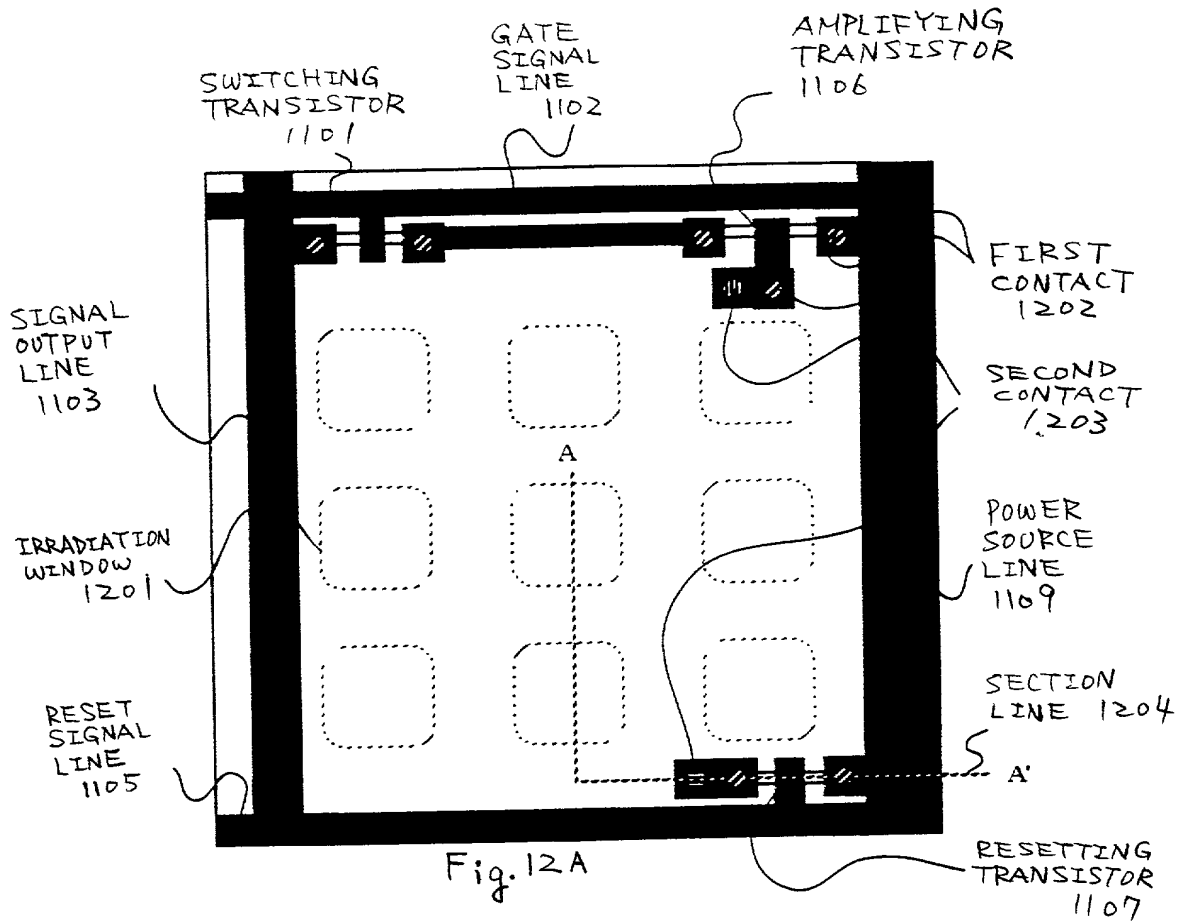
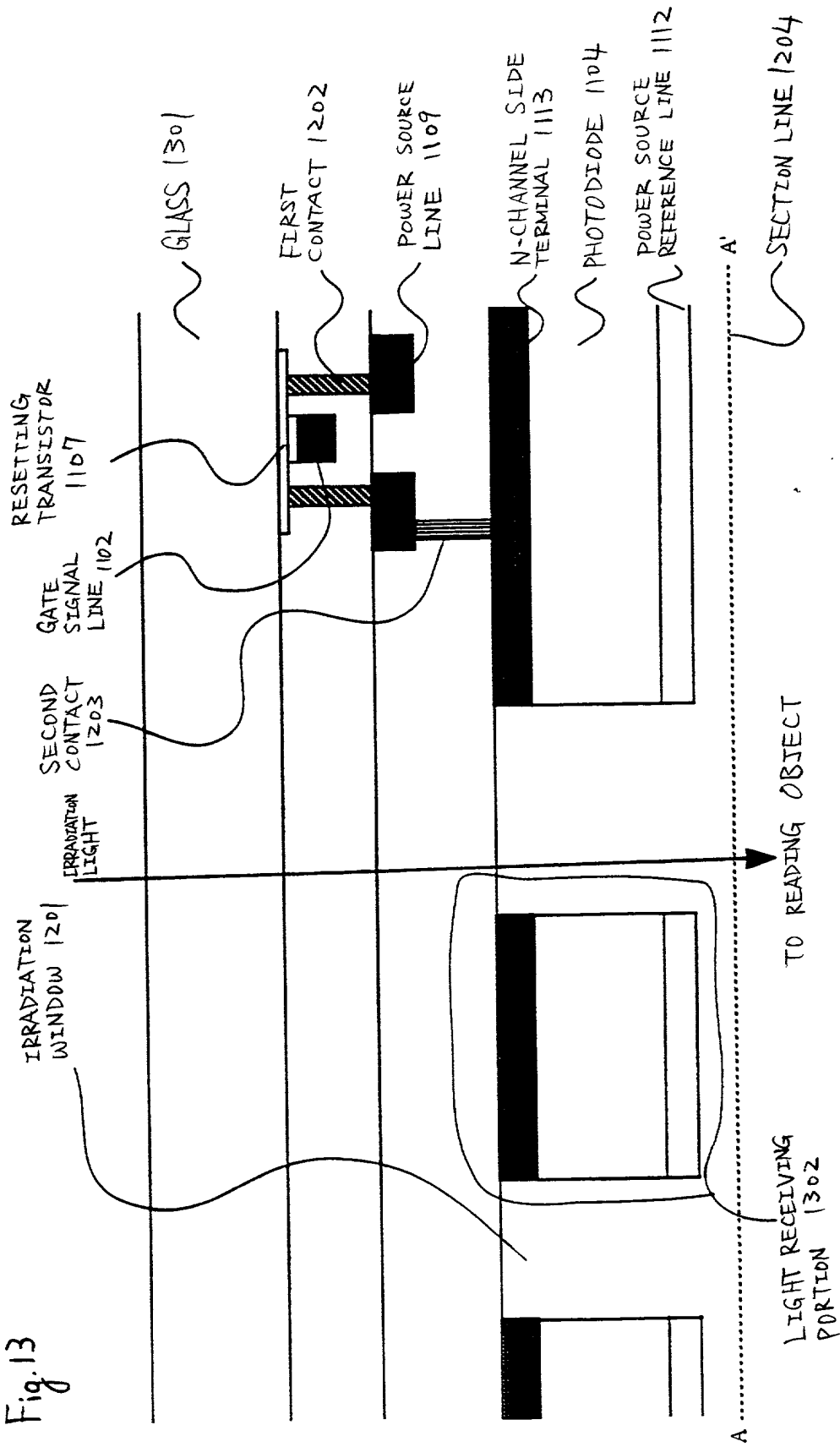


Fig. 13



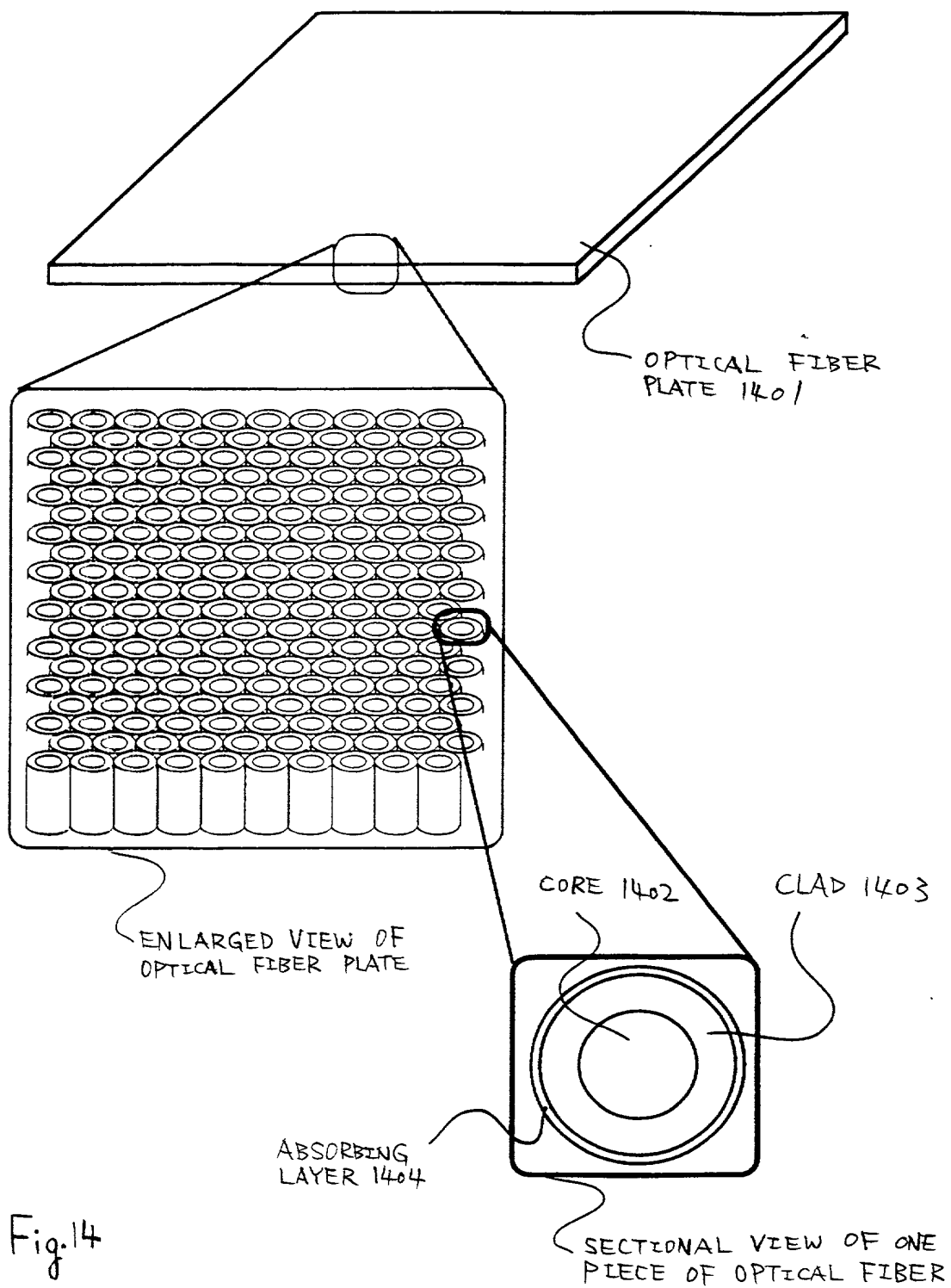


Fig. 14

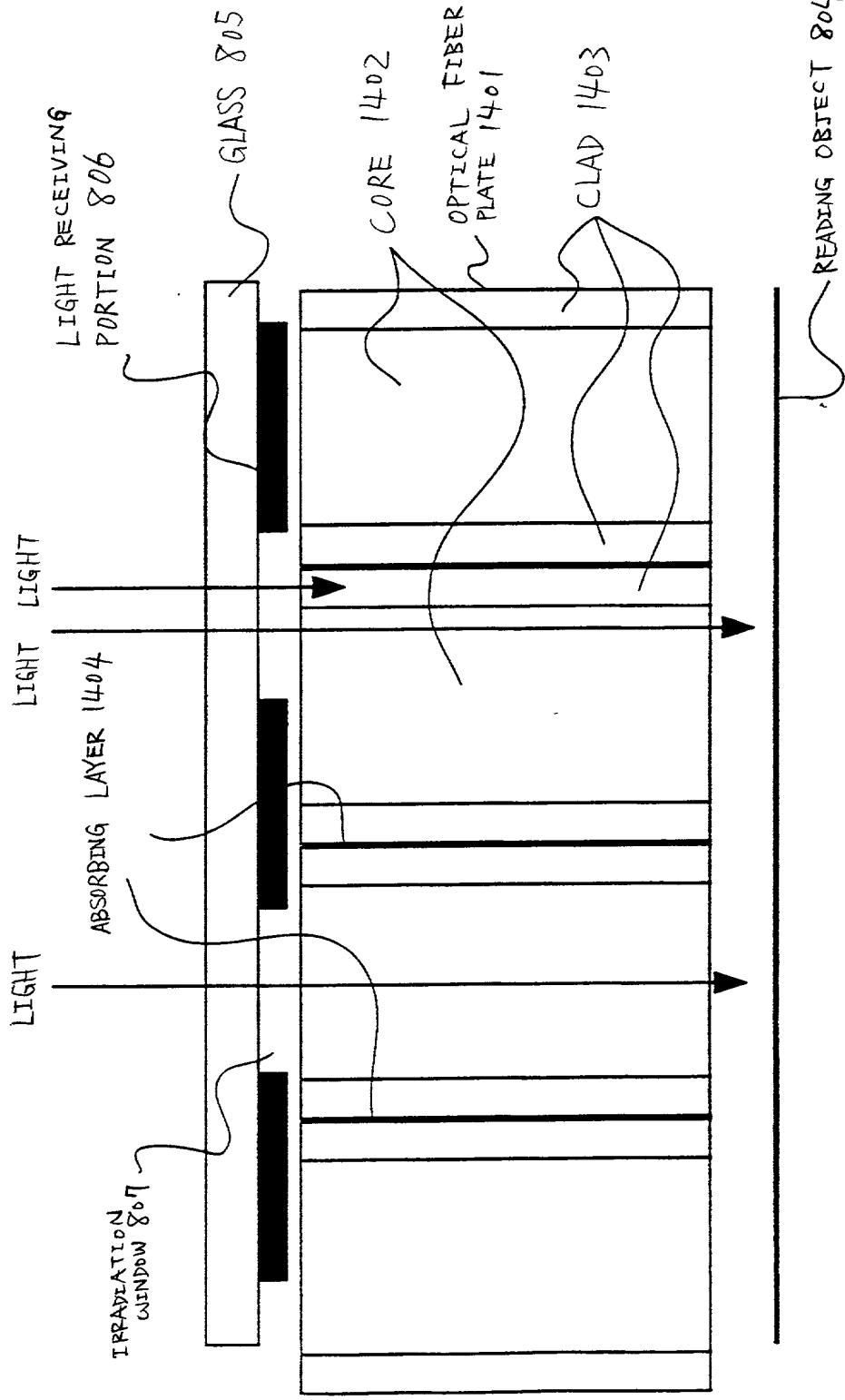


Fig. 15

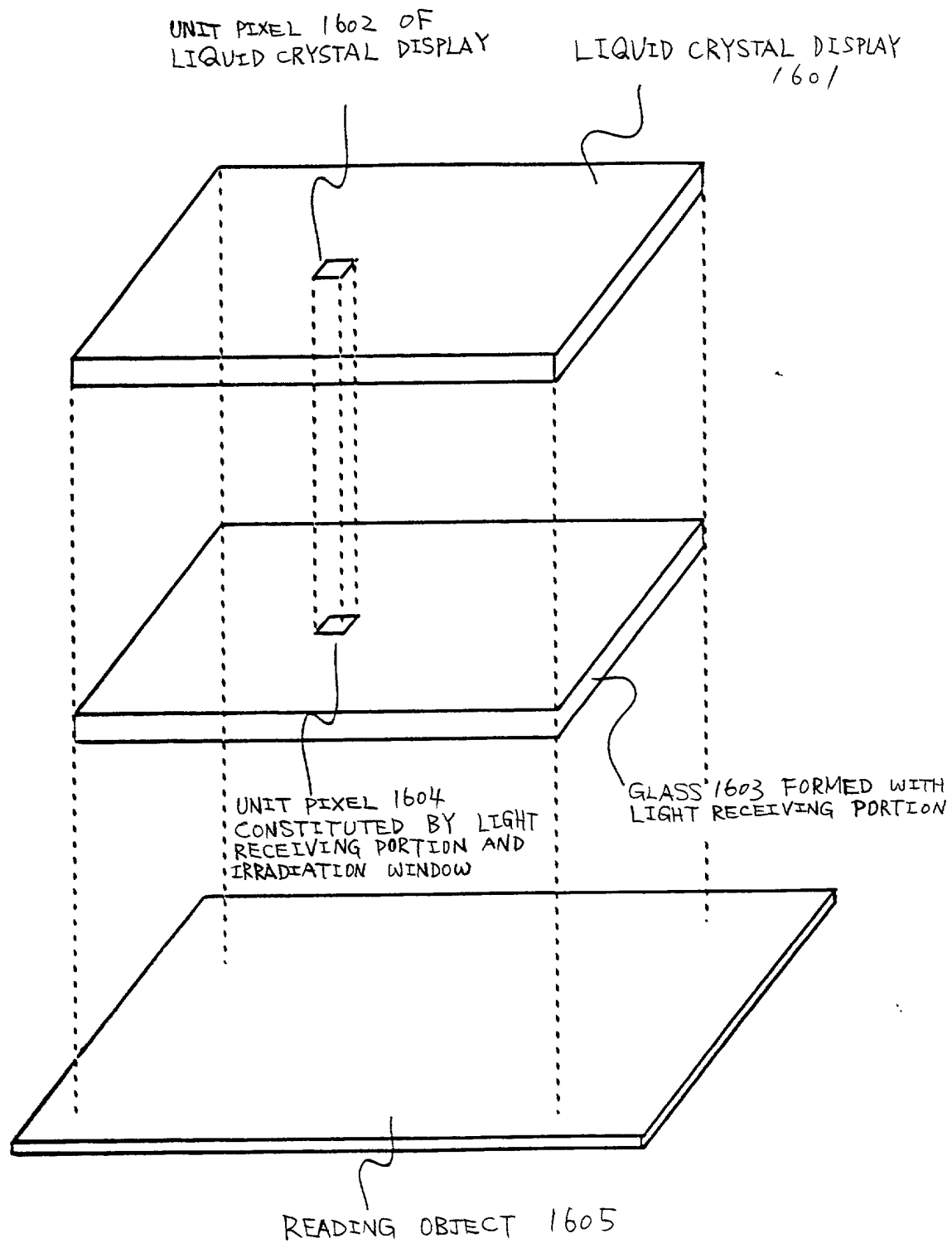


Fig. 16

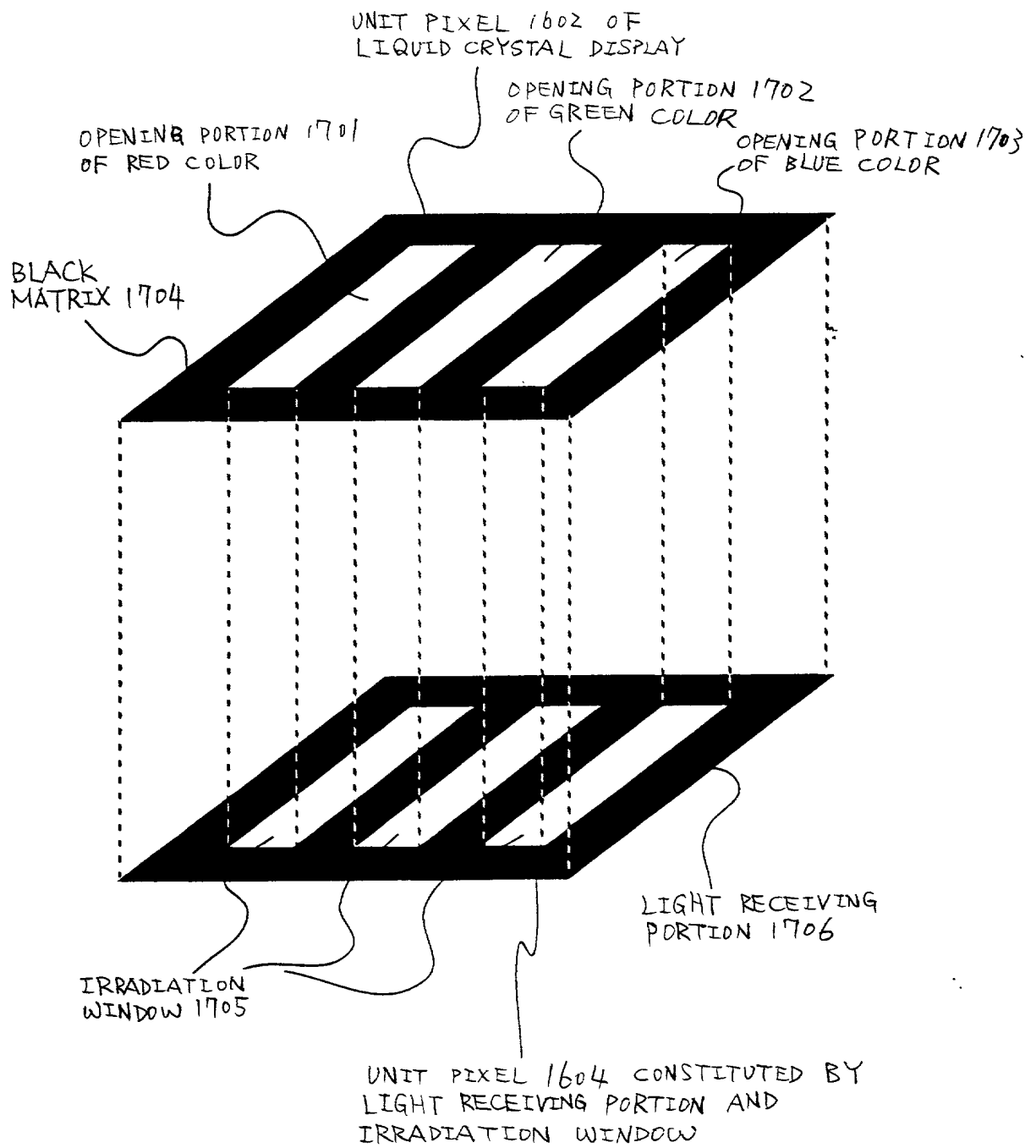
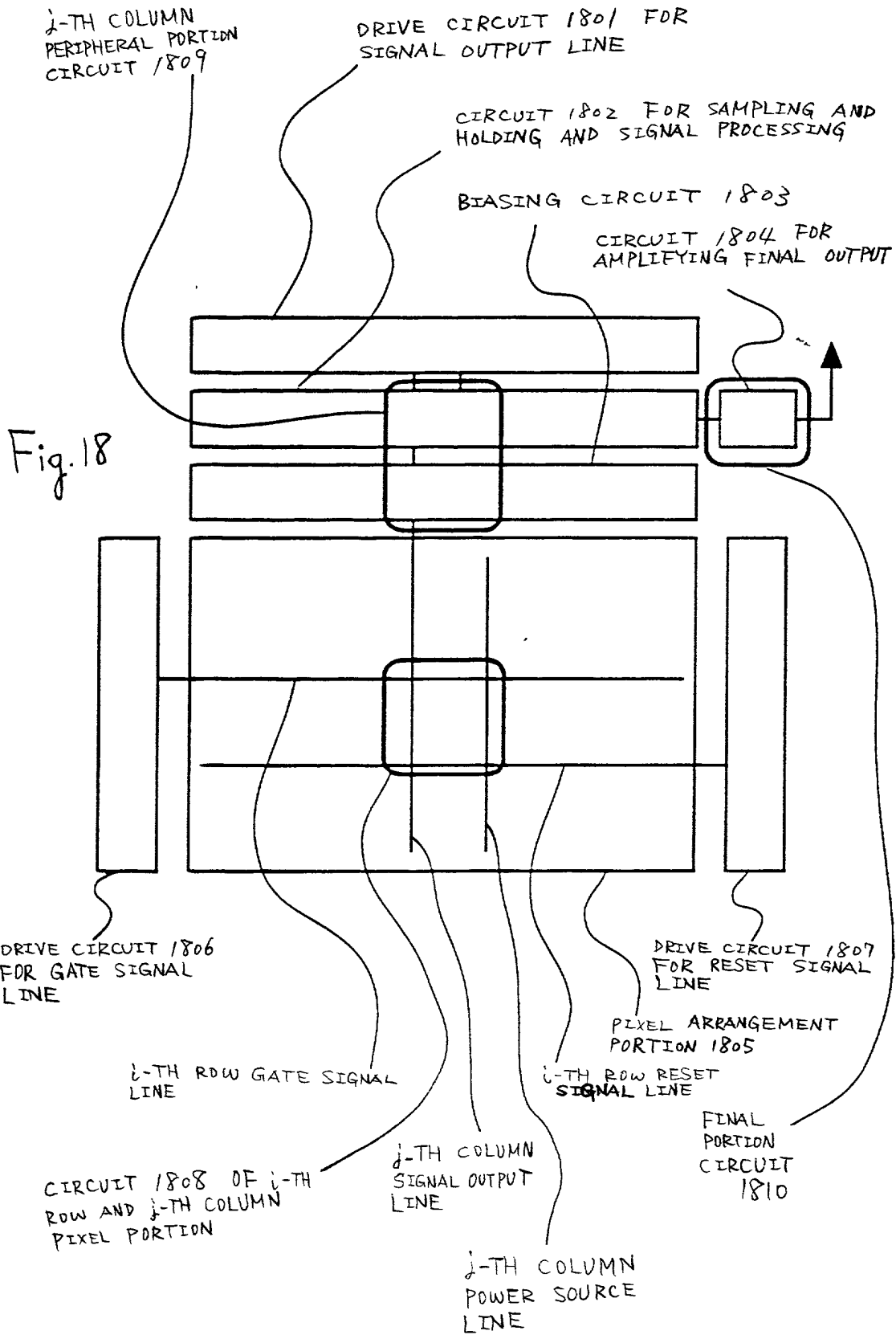


Fig. 17



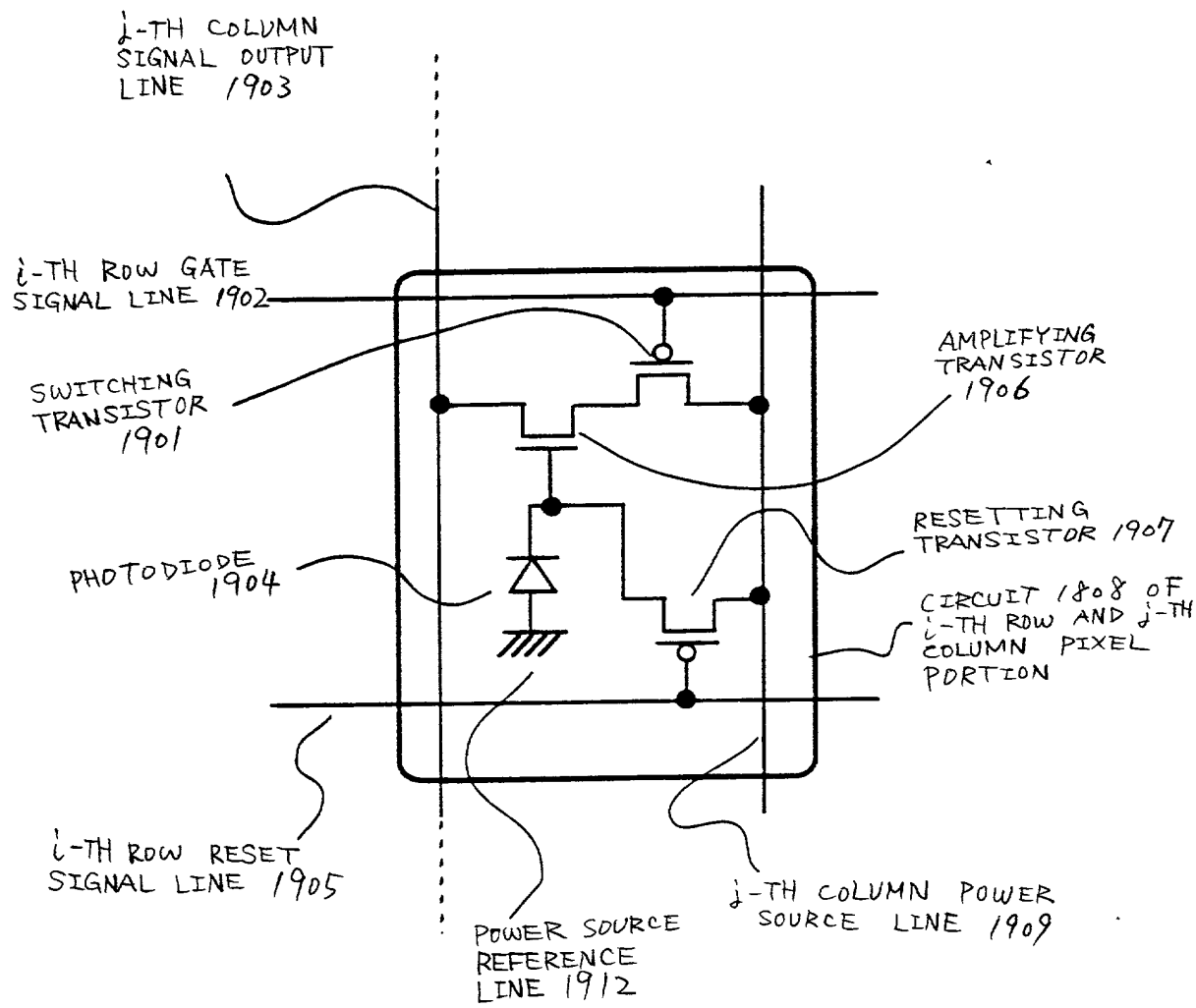


Fig. 19

j -TH ROW SIGNAL
OUTPUT LINE 2003

i -TH ROW GATE
SIGNAL LINE 2002

SWITCHING
TRANSISTOR
2001

PHOTODIODE
2004

i -TH ROW RESET
SIGNAL LINE 2005

AMPLIFYING
TRANSISTOR
2006

RESETTING
TRANSISTOR
2007

j -TH COLUMN POWER
SOURCE REFERENCE
LINE 2012

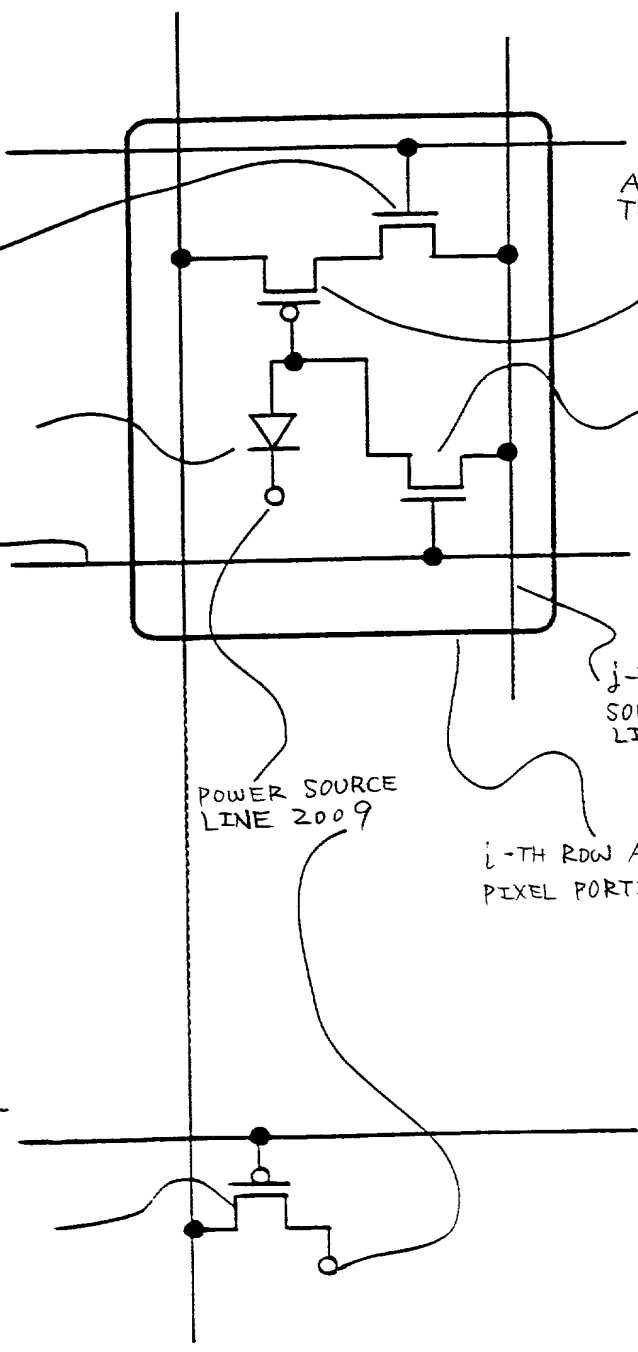
POWER SOURCE
LINE 2009

i -TH ROW AND j -TH COLUMN
PIXEL PORTION CIRCUIT 1808

BIAS SIGNAL
LINE 2010

BIASING
TRANSISTOR
2011

Fig. 20



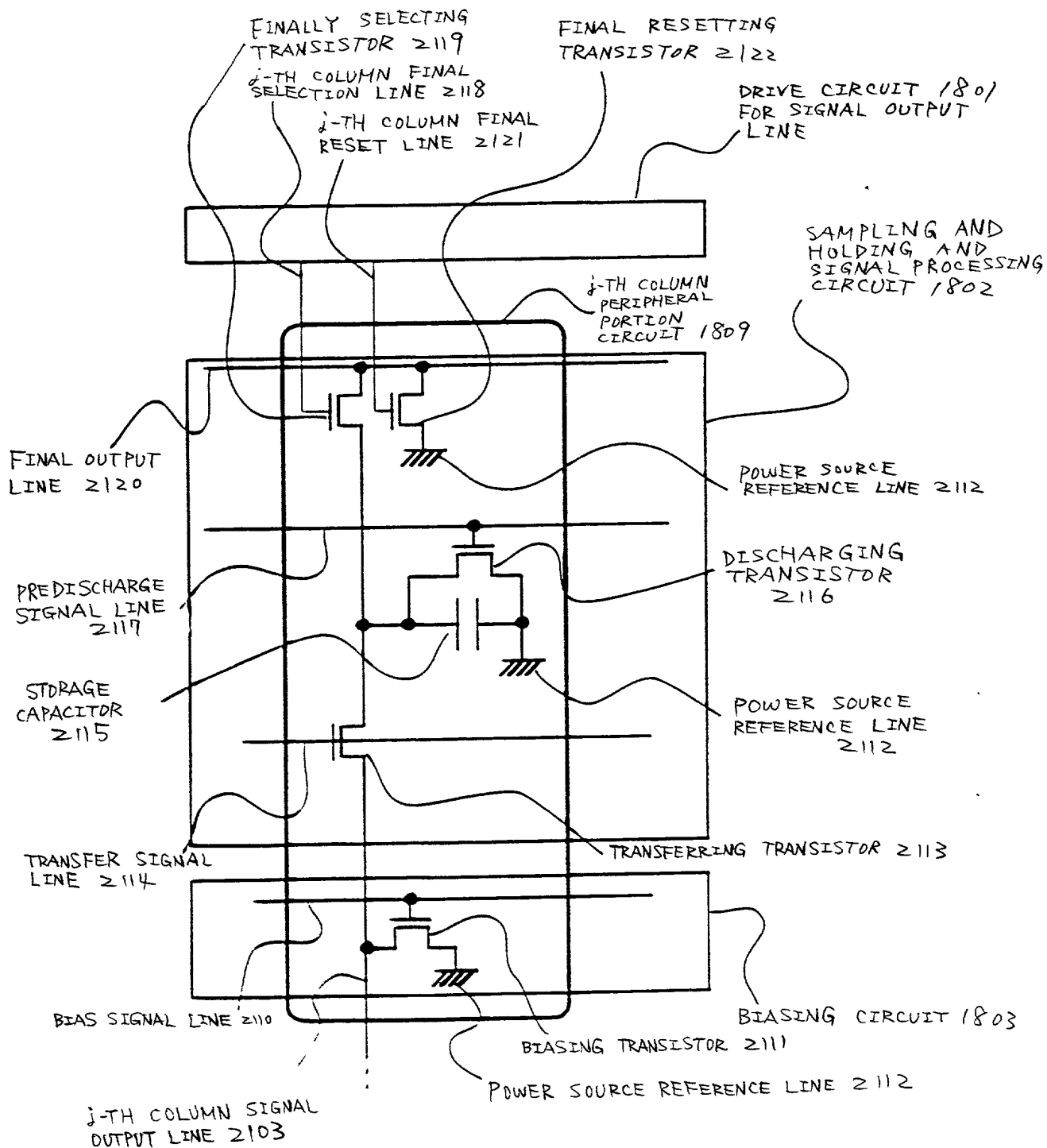


Fig. 21

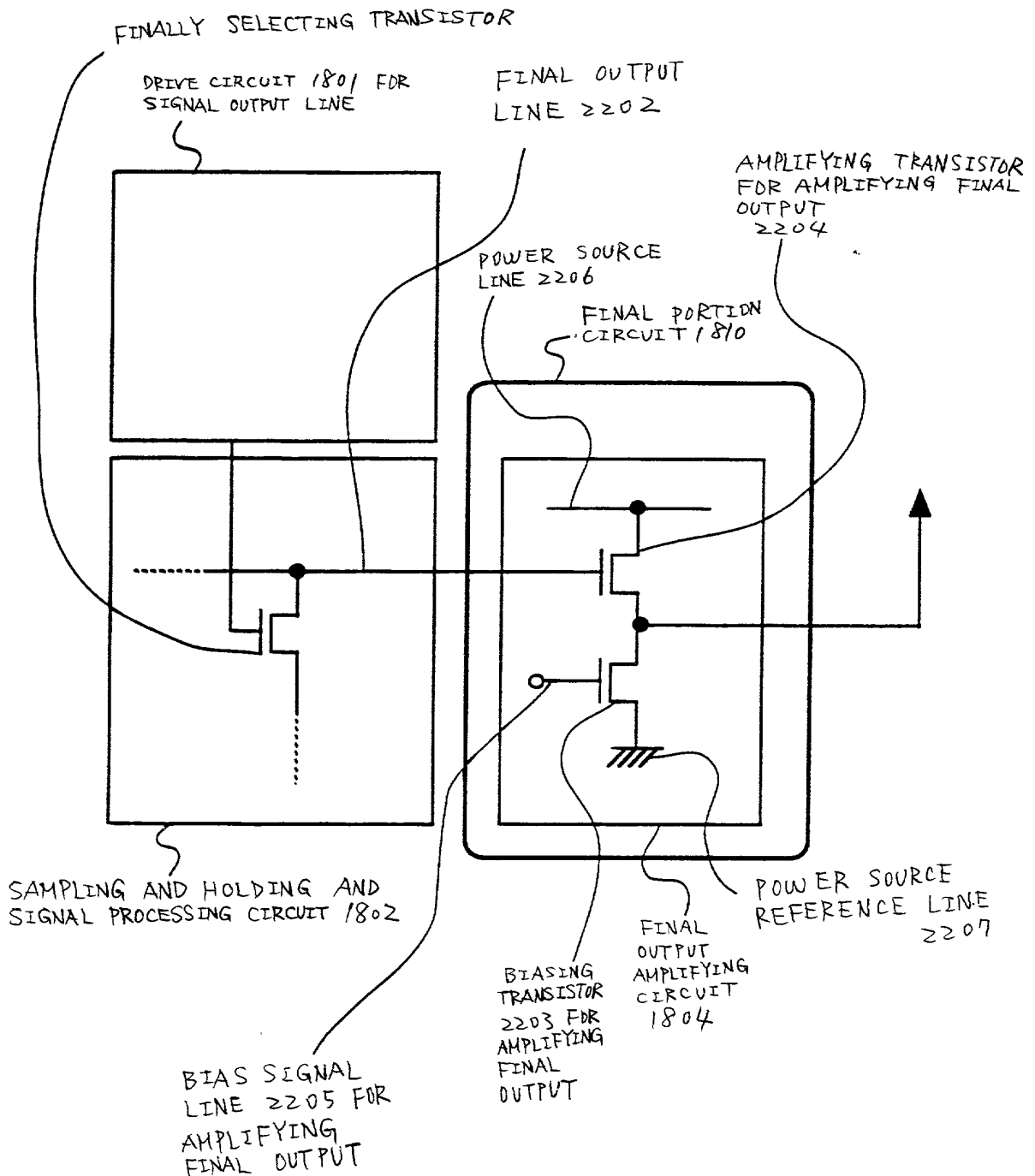


Fig. 22

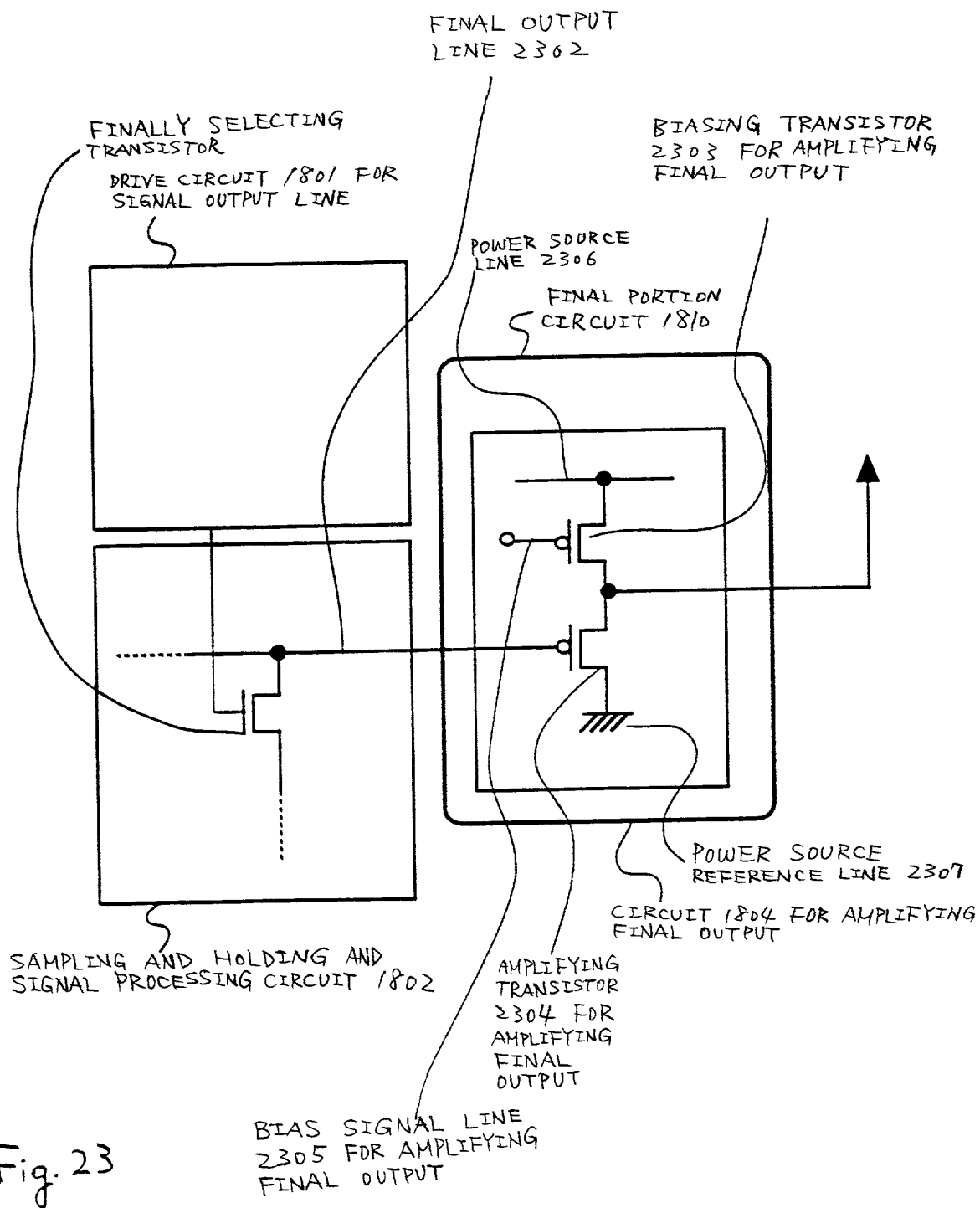
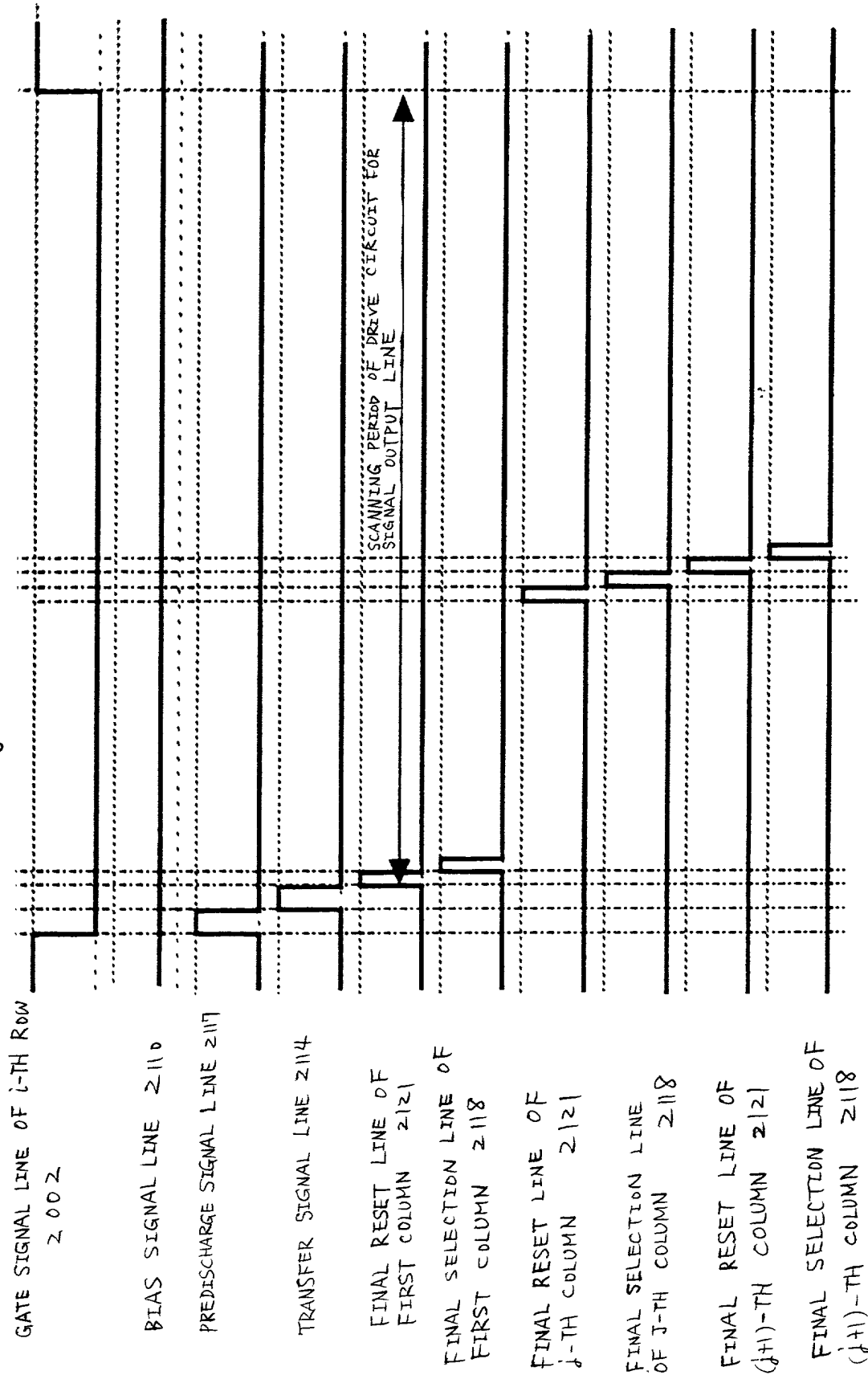


Fig. 23

Fig. 25



CRYSTALLIZATION STEP

Fig. 26A

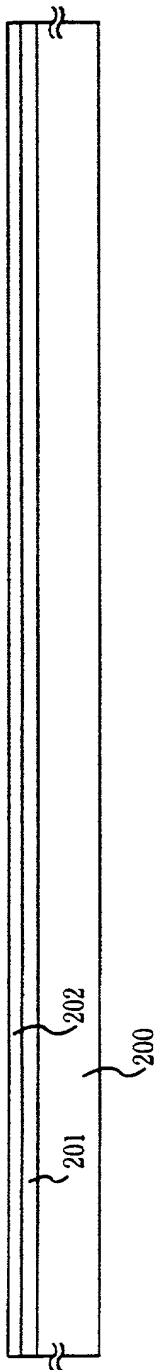
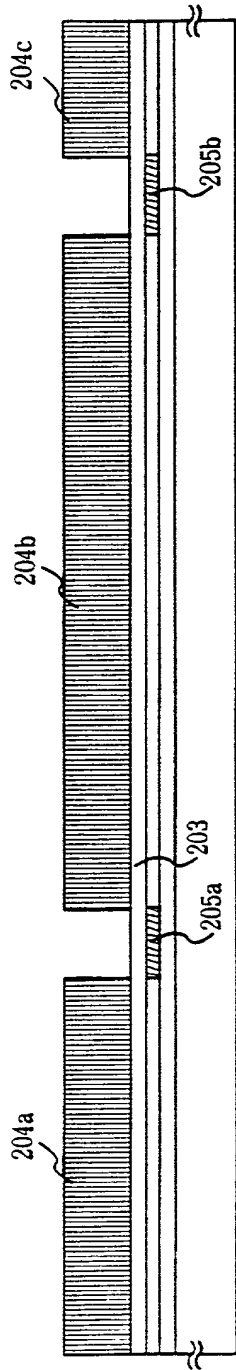


Fig. 26B



LASER ANNEALING STEP

Fig. 26C



Fig. 26D

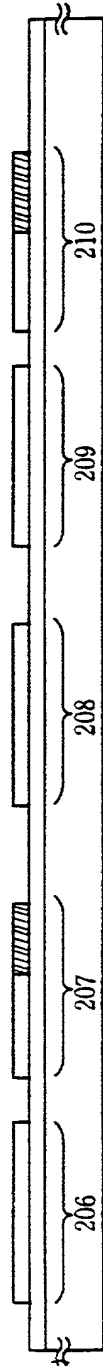


Fig. 27A

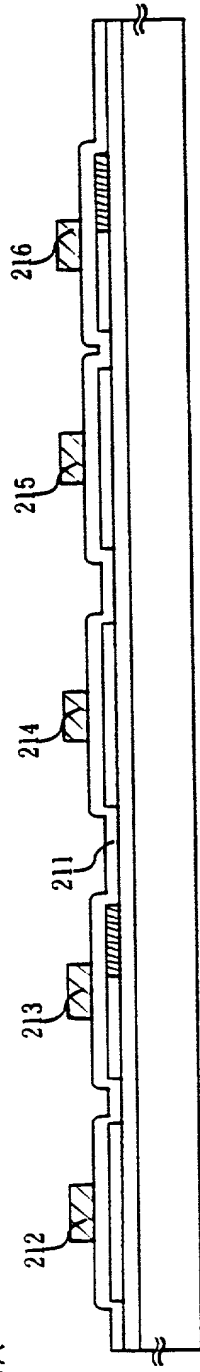


Fig. 27B

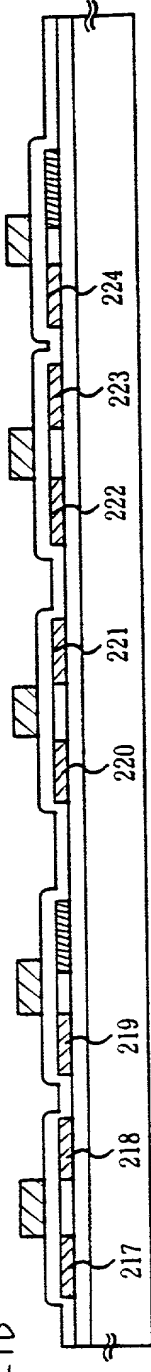


Fig. 27C

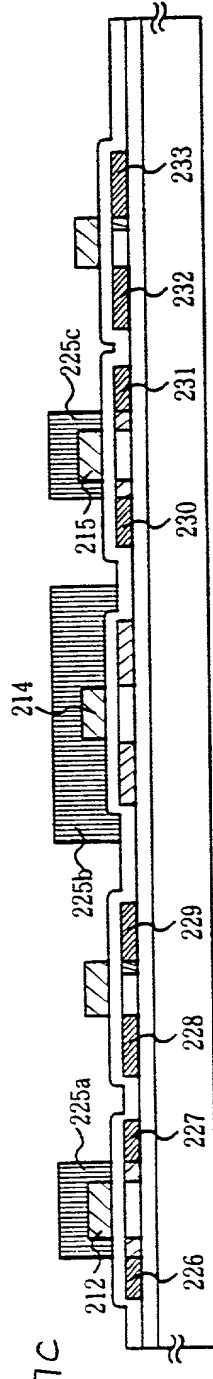
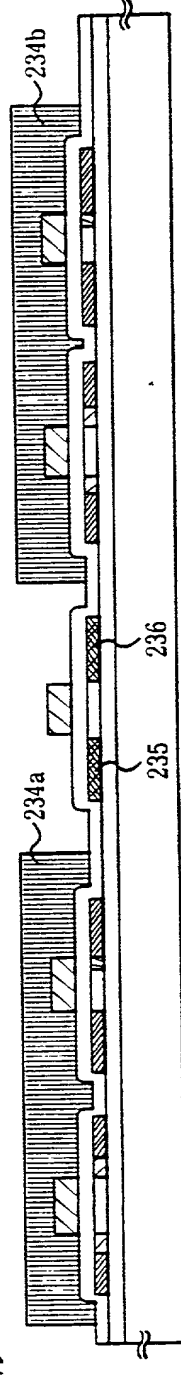


Fig. 27D



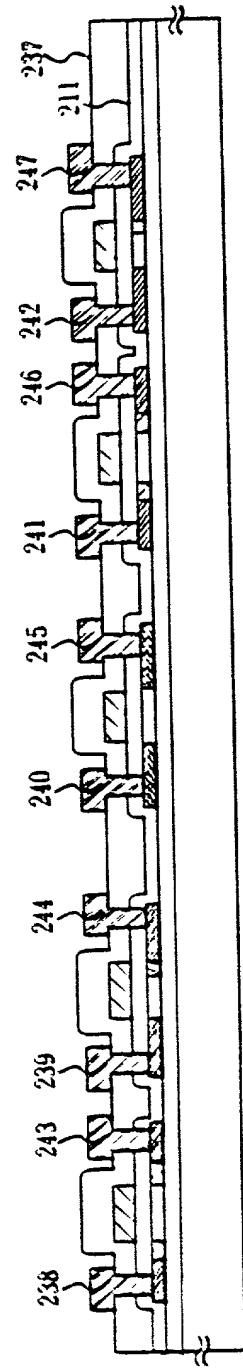


Fig. 28A

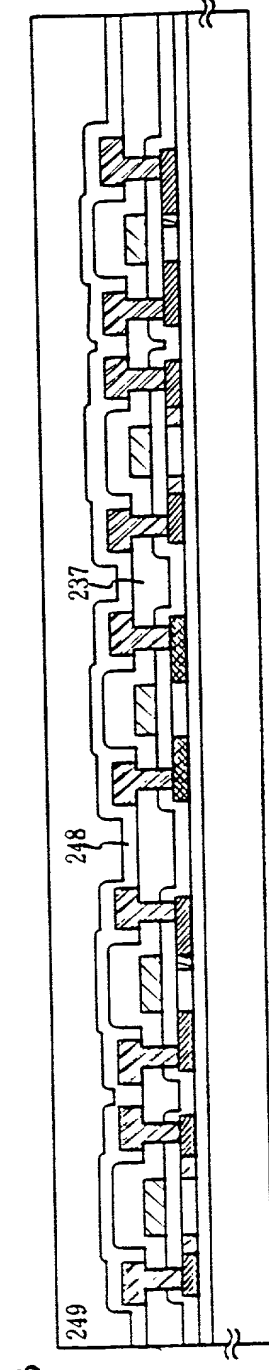


Fig. 28B

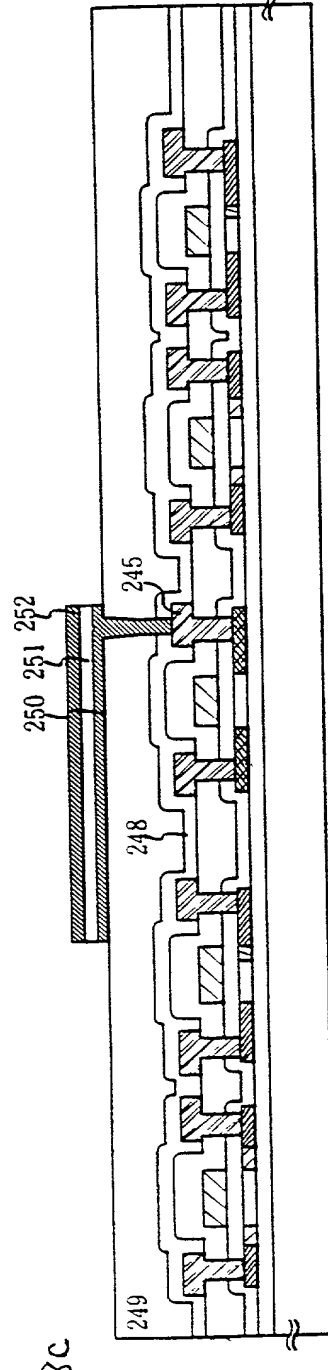


Fig. 28C

This diagram shows a cross-sectional view of a TFT array substrate. A common electrode 260 is formed on the top surface of the substrate. Below it, a series of TFTs are arranged. The TFTs are labeled with their gate, source, and drain electrodes: 212, 213, 215, and 216. The source and drain electrodes are labeled 281, 282, 283, 284, 285, and 286. The TFTs are connected to a common electrode 260. The diagram is divided into four sections by dashed lines, each labeled with a function: "APPLYING TFT 270", "SWITCHING TFT 271", "RESETTING TFT 272", and "BIASING TFT 273". The final section is labeled "DISCHARGE TFT 274".

